IN THE CLAIMS

Please amend the claims as follows:

1. (Previously Presented): A magnetic random access memory comprising:

a tunnel magnetoresistive (TMR) element having first and second TMR layers stacked on each other;

first and second current driving lines configured to generate magnetic fields for storing data to each of said first and second TMR layers, and to cross each other;

said first and second TMR layers are located between said first and second current driving lines; and

a value of a current of said first current driving line is greater than that of said second current driving line when data is written in said second TMR layer, and a value of a current of said second current driving line is greater than that of said first current driving line when data is written in said first TMR layer.

2. (Previously Presented): The magnetic random access memory according to claim 1, further comprising:

a source line; and

a switching element connected between said TMR element and said source line,

wherein said switch element turns on when data is read out from said TMR element.

3. (Previously Presented): The magnetic random access memory according to claim 1,

wherein each of said first and second TMR layers has magnetic layers and an insulating layer between said magnetic layers, and a direction of a spin of one of said magnetic layers is fixed by an antimagnetic layer.

4. (Previously Presented): The magnetic random access memory according to claim 3, wherein said TMR element has a nonmagnetic conductive layer provided between said first and second TMR layers.

5. (Previously Presented): The magnetic random access memory according to claim 3, wherein said antimagnetic layer is provided between said first and second TMR layers.

6. (Previously Presented): The magnetic random access memory according to claim 1, wherein the first current driving line is a bit line and said TMR element is in contact with said bit line.

7. (Previously Presented): The magnetic random access memory according to claim 6, wherein the second current driving line and the bit line are at right angles to each other.

8. (Previously Presented): The magnetic random access memory according to claim 7, wherein said TMR element is in contact with an under surface of said bit line and the second current driving line is provided directly under said TMR element.

9. (Canceled)

10. (Previously Presented): The magnetic random access memory according to claim 2, wherein the second current driving line and the source line are overlapped each other and extend in the same direction.

11. (Previously Presented): The magnetic random access memory according to claim 3, wherein each of said first and second TMR layers stores data based on the direction of the spin of one of said magnetic layers.

12. (Previously Presented): The magnetic random access memory according to claim 1, wherein each of said first and second TMR layers receives a magnetic field intensity dependent on currents of said first and second current driving lines, as a result, the data is written in each of said first and second TMR layers individually.

13. (Previously Presented): The magnetic random access memory according to claim 12, wherein said first and second TMR layers are separated from each other.

14. (Previously Presented): The magnetic random access memory according to claim 1, wherein the asteroid curves of said first and second TMR layers are different from each other and the data is written in each of said first and second TMR layers individually.

15. (Previously Presented): The magnetic random access memory according to claim 14, wherein a data write operation begins with the first TMR layer and ends with the second TMR layer, and a strongest magnetic field intensity is required for the first TMR layer to change the data and a weakest magnetic field intensity is required for the second TMR layer to change the data.

16. (Previously Presented): The magnetic random access memory according to claim 1,

wherein a current of the first current driving line flows in only one direction and a current of the second current driving line flows in one direction or another direction.

17. (Previously Presented): The magnetic random access memory according to claim 3,

wherein a thickness of said insulating layer determines a value of a resistance of each of said first and second TMR layers.

18. (Previously Presented): The magnetic random access memory according to claim 1, further comprising:

a detecting resistance connected to said TMR element,

wherein the data of said TMR element is detected based on a voltage of said detecting resistance in a read operation.

19. (Previously Presented): The magnetic random access memory according to claim 18,

wherein said detecting resistance is provided at an outer portion of a memory cell array portion.

20. (Previously Presented): The magnetic random access memory according to claim 18, further comprising:

the power source electrically connected to said TMR element in a read operation and generates a read current.

21-53. (Canceled)

54. (Previously Presented): The magnetic random access memory according to claim 1, further comprising:

a register temporarily latches the data having a plurality of bits.

55-56. (Canceled)

57. (New): The magnetic random access memory according to claim 7,

wherein said TMR element is contact with an upper surface of said bit line and the second current driving line is provided directly above said TMR element.